Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled)

Claim 2 (currently amended): ~~**The semiconductor memory device of Claim 1**~~ **A semiconductor memory device comprising:**

a semiconductor substrate;

a dielectric gate stack formed on a channel region of the substrate, the dielectric gate stack having a top portion and a bottom portion;

the dielectric gate stack including an electron trapping layer formed of an ~~**wherein the**~~ electron trapping material **that** is selected from among the group consisting of zirconium oxide~~**, hafnium oxide,**~~ and aluminum oxide.

Claim 3 (withdrawn). The semiconductor memory device of Claim 2 wherein the dielectric gate stack is comprised entirely of the electron trapping layer.

Claim 4 (original): The semiconductor memory device of Claim 2 wherein the dielectric gate stack includes a first layer of dielectric material and a second layer of dielectric material configured such that the first layer of dielectric material is formed on the channel region of the substrate and the electron trapping layer is formed on the first layer of dielectric material and wherein the second layer of dielectric material is formed on the electron trapping layer.

Claim 5 (original): The semiconductor memory device of Claim 4 wherein the first layer of dielectric material and the second layer of dielectric material are each comprised of silicon dioxide.

Claim 6 (original): A memory device as in Claim 4 wherein the first layer of dielectric material is formed of a different dielectric material than the second layer of dielectric material.

Claim 7 (withdrawn). The semiconductor memory device of Claim 1 wherein the dielectric gate stack is comprised entirely of the electron trapping layer that comprises zirconium oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Zr_xSi_yO_z$.

Claim 8 (withdrawn). The semiconductor memory device of Claim 1 wherein the dielectric gate region is comprised entirely of the electron trapping layer that comprises aluminum oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Al_xSi_yO_z$.

Claim 9 (withdrawn). The semiconductor memory device of Claim 1 wherein the dielectric gate region is comprised entirely of the electron trapping layer that comprises hafnium oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Hf_xSi_yO_z$.

Claim 10 (currently amended): A semiconductor integrated circuit having the memory devices of Claim 2 [[1]] formed thereon.

Claim 11 (currently amended): A semiconductor memory device comprising:

a semiconductor substrate having a source and a drain separated by a channel region;

a first dielectric layer formed on a channel region of the substrate;

an electron trapping layer formed on the first dielectric layer, **the electron trapping layer formed of an electron trapping material that is selected from among the group consisting of zirconium oxide and aluminum oxide**;

a second dielectric layer formed on the electron trapping layer; and

a gate electrode connected with the second dielectric layer.

Claim 12 (withdrawn): A method for forming a memory device comprising:

providing a semiconductor substrate;

forming a gate stack over a channel region of the substrate such that the gate stack includes a layer of electron trapping material; and

forming a gate electrode connected with a top portion of the gate stack.

Claim 13 (withdrawn): The method for forming a memory device as in Claim 12, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

Claim 14 (withdrawn): The method for forming a memory device as in Claim 12 wherein forming the gate stack comprises forming a first layer of dielectric material over the channel region of the substrate and forming the layer of electron trapping material over the first layer of dielectric material and forming a gate electrode connected with the layer of electron trapping material.

Claim 15 (withdrawn): The method for forming a memory device as in Claim 14, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

Claim 16 (withdrawn): The method for forming a memory device as in Claim 15, wherein forming the first layer of dielectric material comprises formed the first layer of dielectric material with a silicon oxide material.

Claim 17 (withdrawn): The method for forming a memory device as in Claim 12 wherein forming the gate stack comprises:

forming a first layer of dielectric material over the channel region of the substrate;

forming the layer of electron trapping material over the first layer of dielectric material;

forming a second layer of dielectric material over the layer of electron trapping material; and

forming a gate electrode connected with a top portion of the second layer of dielectric material.

Claim 18 (withdrawn): A method for forming a memory device as in Claim 17, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping

material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

Claim 19 (withdrawn): The method for forming a memory device as in Claim 18, wherein forming the first layer of dielectric material and forming the second layer of dielectric material comprises formed the first layer of dielectric material and the second layer of dielectric material with a silicon oxide material.

Claim 20 (withdrawn): The method for forming a memory device as in Claim 18, wherein forming the first layer of dielectric material and forming the second layer of dielectric material comprises formed the first layer of dielectric material and the second layer of dielectric material with different dielectric material.